LINE INTERFACE, MODE 3 (LI-3), 628060

GENERAL DESCRIPTION

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1. GENERAL

1.01 This Section provides a general description of the ITT D448 line interface, Mode 3 (LI-3), 628060 (Fig. 1), to the functional block diagram level.

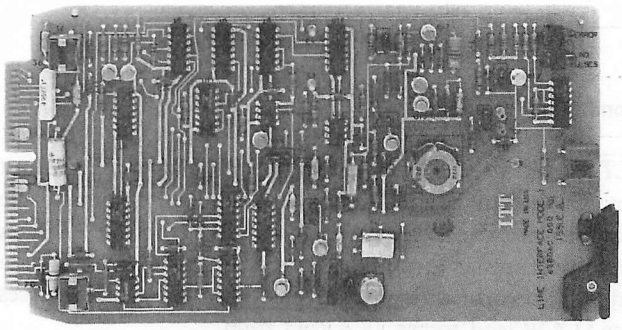

Fig. 1—LI-3, 628060

1.02 Whenever this Section is reissued, the reasons for reissue will be listed in this paragraph.

1.03 The LI-3 interfaces one digroup (24 channels) of a D448 Mode 3 multiplex terminal to the incoming and outgoing 1.544 Mb/s (T1) lines.

2. DESCRIPTION

2.01 The unit mounts in the D448 multiplex shelf (common equipment mounting section) in connector J7C (for Digroup A) or J8C (for Digroup B). Installation procedures for the unit are provided in Section ITTR-18-433.

2.02 The unit is available in Group -0 only.

2.03 The unit consists of an epoxy-glass printed circuit board (PCB) and associated circuit components. The lower front edge of the PCB is fitted with a handle to facilitate insertion and removal of the unit from the shelf. An identification strip on the handle face indicates the unit mnemonic (LI-3), last three digits of the model number, last three digits of the part number, and issue letter. The part number and issue letter are also located on the component side of the PCB directly behind the handle.

2.04 The ERROR and NO PULSES LEDs and the LOOP test points are located on the front edge of the PCB.

2.05 Printed circuit wiring is etched on both sides of the PCB. Unit inputs and outputs are terminated in gold-plated contacts on the rear edge of the PCB. These contacts mate with a 70-pin contact edge connector on the rear of the multiplex shelf.

3. FUNCTIONAL OPERATION (FIG. 2)

TRANSMIT SIDE

3.01 The 1.544-MHz oscillator generates a 1.544-MHz signal which is applied to the clock selector. The clock selector selects either an external clock or the generated clock to synchronize the digroup. The external clock may be selected only when an office interface unit (OIU) is used in the system. When the OIU sets the SELECT lead low, clock from the OIU on the TCL1544L lead is selected to be the clock signal for the transmit side. The clock selector applies the selected clock to the transmit (TX) data latch and to the transmit logic unit (TLU) on the TCL1544 lead. The TLU distributes the clock to the transmit portion of the digroup for synchronization.

3.02 The incoming unipolar data from the TLU is applied to the TX data latch on the TD1544 lead and is latched by the clock and applied to the alternate mark inversion (AMI) converter. The incoming unipolar

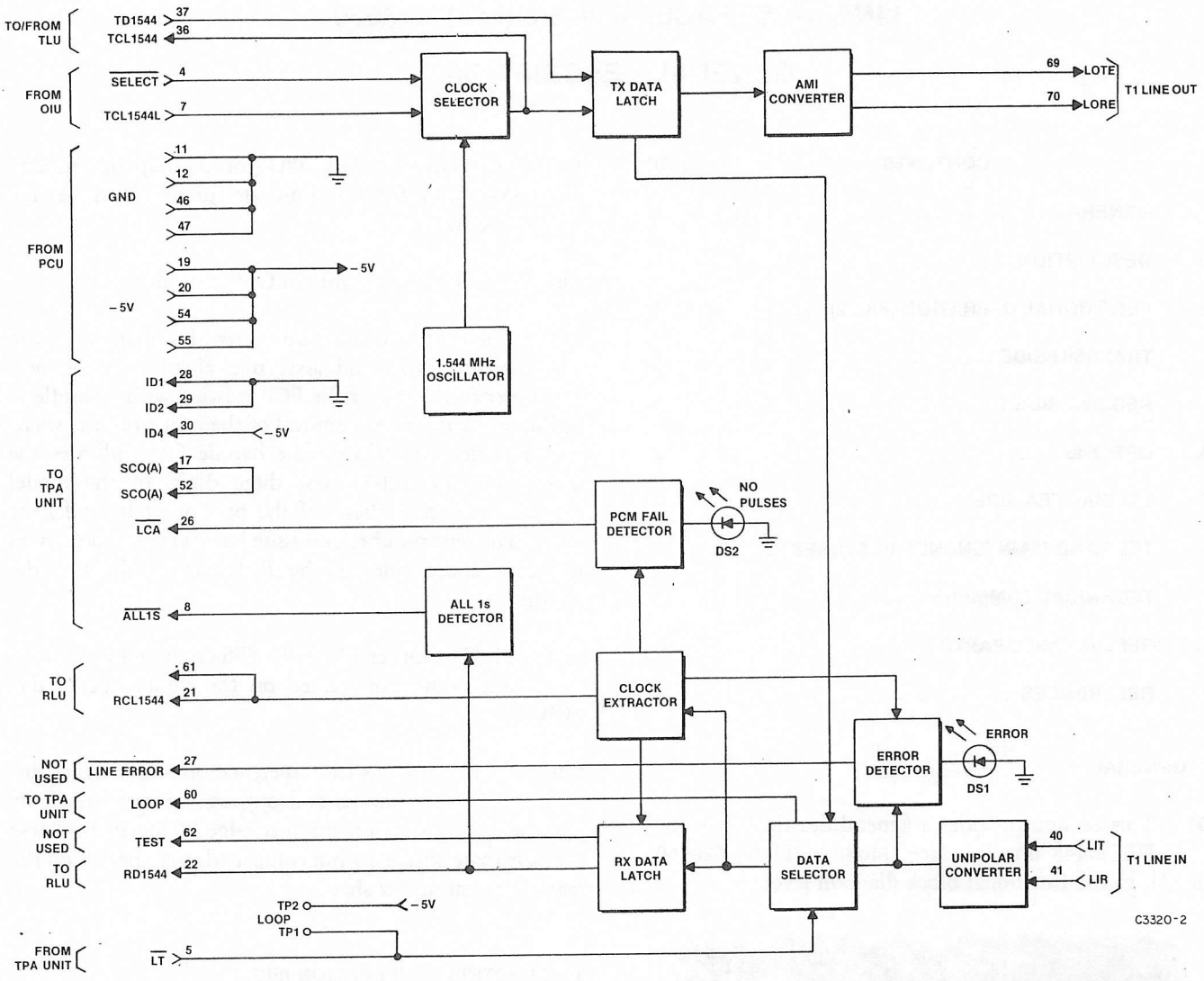

Fig. 2—LI-3, 628060, Functional Block Diagram

data is also applied to the data selector, which selects this data when the digroup is looped.

3.03 The AMI converter converts the incoming unipolar data to bipolar data. The bipolar output of the AMI converter is applied to the central office equalizer (EQL) on the LOTE and LORE leads.

RECEIVE SIDE

3.04 T1 bipolar data is applied to the unipolar converter on the LIT and LIR leads. The unipolar converter converts the data from bipolar to unipolar and applies it to the data selector and to the error detector.

3.05 During normal operation (digroup not looped), the data selector selects the incoming data from the unipolar converter and applies it to the clock extractor and the receive (RX) data latch. When the digroup is looped ($\overline{LT}$ lead from the trunk processor and alarm (TPA) unit low or shorting plug inserted in LOOP test points), the data selector selects the TX unipolar data from the TX data latch and applies it to the clock extractor and the RX data latch. When the digroup is looped, the data selector forces the LOOP lead to the TPA unit high.

3.06 The clock extractor recovers the 1.544-MHz clock from the incoming data. The clock extractor applies the recovered clock to the receive logic unit (RLU) on the RCL1544 lead to synchronize the receive portion of the digroup. The recovered clock is also applied to the RX data latch, the error detector, and the PCM fail detector.

3.07 The RX data latch samples and latches the selected data to the recovered clock and outputs the RX data to the RLU on the RD1544 lead. The output of the RX data latch is also applied to the all 1s detector.

3.08 The error detector samples the incoming unipolar data for errors. If two consecutive bits are of the same polarity, the error detector turns on the ERROR LED and forces the LINE ERROR lead low. The error detector is disabled during looped operation.

3.09 The PCM fail detector monitors the output of the clock extractor to check for the presence of incoming data. If incoming data is not present, the clock extractor will not apply recovered clock to the PCM fail circuit. The PCM fail detector turns on the NO PULSES LED and forces the LCA lead to the TPA unit low to cause a local alarm.

3.10 The all 1s detector monitors the output of the RX data latch for the remote alarm indication (all 1s) from the far-end digroup. If the data is all 1s, the ALL1S lead to the TPA unit is forced low to cause a remote alarm.

4. OPTIONS

4.01 This unit has no field-selectable options. However, strapping options on the backplane of the multiplex shelf control clock synchronization. Refer to Section ITTR-18-405 for option selection information on these strapping options.

5. SPECIAL FEATURES

5.01 If the LI-3 is removed from the multiplex shelf while the terminal is in service, a local alarm will occur. The SCO loop on the unit is fed to the TPA unit; if that loop opens, the TPA unit causes a local alarm.

6. TEST AND MAINTENANCE FEATURES

6.01 A description of the test and maintenance features of the unit is provided in Table A. Refer to Fig. 1 for the physical location of these features.

TABLE A

FEATURE	REF. DES.	FUNCTION
ERROR LED	DS1	Turns on when bipolar errors are detected in incoming data.
NO PULSES LED	DS2	Turns on when incoming data is not present.

TABLE A (CONT)

FEATURE	REF. DES.	FUNCTION
LOOP test points	TP1 & TP2	Provides a means of looping the digroup when the digroup is not in trunk processing.

6.02 The looping initiated at the TPA unit requires that the digroup be in a carrier group alarm (CGA) condition, and while looped the CGA condition cannot be cleared. The alternate looping method provided by the LOOP test points is called the LI- loop. This LI- loop, initiated by the insertion of a shorting plug in the LOOP test points, does not necessitate a CGA condition as opposed to the digroup looping. The intent of the LI- loop is to provide for "hot-standby" operation between system installation and final system turn-up, should that be an extended period of time. During LI- loop, the alarm reporting is active and all channel unit signaling highways are available for testing purposes.

7. TECHNICAL SUMMARY

7.01 A summary of technical specifications for the unit is given in Table B.

TABLE B

ITEM	SPECIFICATION
DC POWER	
Voltage Current	−5 ±0.25 Vdc 150 mA nominal, 250 mA maximum
T1 LINE OUTPUT	
Line Rate Line Code Output Impedance Pulse Characteristics Base to Peak Height Negative and Positive Pulse Unbalance Half-Amplitude Width Maximum Rise and Fall Time Trailing Edge Overshoot	1.544 Mb/s ±200 b/s Bipolar 100 ohms nominal 6 ±0.6V ±0.3V, ±15 ns 324 ±30 ns 80 ns 30 ±10% of pulse height, decaying to 10% or less of base line within 400 ns

TABLE B (CONT)

ITEM	SPECIFICATION
T1 LINE INPUT	
Line Rate Line Code Input Impedance Amplitude Minimum Pulse Density	1.544 Mb/s ± 200 b/s Bipolar 100 ohms nominal ± 1.5 to ± 3V 15 consecutive zeros
OPERATING ENVIRONMENT	
Temperature Humidity Altitude	0° to 55°C To 95% at 40°C (no condensation) 14,000 ft (4,267 m)
DIMENSIONS	
Height Width Depth	5.0 in. (12.7 cm) 0.5 in. (1.3 cm) 9.6 in. (24.4 cm)
WEIGHT	0.4 lb (0.2 kg)

8. REPLACEABLE PARTS

8.01 This unit has no field-replaceable parts.

9. REFERENCES

9.01 The engineering drawings noted in Table C were used in the preparation of this Section.

TABLE C

TYPE	DRAWING NO.
Assembly Schematic	628060-000 628060-002

9.02 Related information on the LI-3 may be found in the ITTR Sections referenced in Table D.

TABLE D

TITLE	SECTION NO.
Connectorized Multiplex Shelf (MS/WC7, MS/WC5, (MS/C7 and MS/C6), 628001, 628005, 628011 and 628015 — General Description	ITTR-18-005
Connectorized Multiplex Shelf (MS/WC7, MS/WC5, MS/C7 and MS/C6), 628001, 628005, 628011 and 628015 — Option Selection, Installation and Pretest	ITTR-18-405
Mode 3 Common Equipment — Installation and Pretest	ITTR-18-433